WHAT IS CLAIMED:

1. An integrated circuit, comprising:

functional circuitry;

a region devoid of the functional circuitry; and

a transistor disposed in the region.

2. The integrated circuit of claim 1 wherein:

the functional circuitry comprises functional-circuit blocks that are spaced apart from one another; and

the devoid region comprises a region that is disposed between the functional-circuit blocks.

3. The integrated circuit of claim 1 wherein:

the functional circuitry comprises a functional-circuit block having a portion devoid of functional-circuit elements; and

the devoid region comprises the devoid portion of the functional-circuit block.

4. The integrated circuit of claim 1 wherein the transistor comprises an FET transistor.

5. The integrated circuit of claim 1 wherein the transistor is automatically placed in the devoid region.

6. The integrated circuit of claim 1 wherein the transistor is manually placed in the devoid region.

7. An integrated circuit, comprising:

functional circuitry;

a region devoid of the functional circuitry; and

a buffer disposed in the region.

8. An integrated circuit, comprising:

functional circuitry;

a region devoid of the functional circuitry; and

a logic circuit disposed in the region.

9. The integrated circuit of claim 8 wherein the logic circuit comprises a logic gate.

10. The integrated circuit of claim 8 wherein the logic circuit comprises an inverter.

11. An integrated circuit, comprising:
first and second supply nodes;
functional circuitry;
a region devoid of the functional circuitry; and
a transistor disposed in the region and having a pair of input-output terminals coupled to the first supply node and having a control terminal coupled to the second supply node.

12. The integrated circuit of claim 11 wherein:
the transistor comprises an FET transistor;
the pair of input-output terminals comprises a pair of source-drain terminals; and
the control terminal comprises a gate terminal.

13. An integrated circuit, comprising:
a conductive path;
functional circuitry;
a region devoid of the functional circuitry; and
a transistor disposed in the region and having a pair of input-output terminals coupled to the conductive path and having a control terminal.

14. The integrated circuit of claim 13, further comprising:
a supply node; and
wherein the control terminal is coupled to the supply node.

15. The integrated circuit of claim 13 wherein the control terminal is coupled to one of the input-output terminals.

16. The integrated circuit of claim 13 wherein the control terminal is short-circuited to one of the input-output terminals.

17. An integrated circuit, comprising:
first and second regions;
functional circuitry disposed in the first and second regions;
a third region devoid of the functional circuitry;
a buffer disposed in the third region and having an input terminal and an output terminal;
a first conductive path having a first terminal coupled to the functional circuitry in the first region and having a second terminal coupled to the input terminal of the buffer; and
a second conductive path having a first terminal coupled to the output terminal of the buffer and having a second terminal coupled to the functional circuitry in the second location.

18. The integrated circuit of claim 17 wherein the functional circuitry in the first and second regions respectively comprises first and second blocks of the functional circuitry, the first and second blocks being spaced apart from one another.

19. The integrated circuit of claim 17, further comprising:
a supply node; and
wherein the buffer comprises a transistor disposed in the devoid region and having a control terminal coupled to the input terminal of the buffer, a first terminal coupled to the output terminal of the buffer, and a second terminal coupled to the supply node.

20. An integrated circuit, comprising:
first and second regions;
functional circuitry disposed in the first and second regions;
a third region devoid of the functional circuitry;
a logic circuit disposed in the third region and having an input terminal and an output terminal;
a first conductive path having a first terminal coupled to the functional circuitry in the first region and having a second terminal coupled to the input terminal of the logic circuit; and

a second conductive path having a first terminal coupled to the output terminal of the logic circuit and having a second terminal coupled to the functional circuitry in the second location.

21. An integrated circuit, comprising:

functional circuitry;

a region devoid of the functional circuitry; and

a repair transistor disposed in the region and having a three terminals, one of the terminals coupled to the functional circuitry.

22. The integrated circuit of claim 21 wherein two of the transistor terminals are coupled to the functional circuitry.

23. The integrated circuit of claim 21 wherein the three transistor terminals are coupled to the functional circuitry.

24. A method, comprising:

identifying an integrated-circuit region that is devoid of a circuit; and

placing a transistor in the devoid integrated-circuit region.

25. The method of claim 24 wherein identifying the devoid integrated-circuit region and placing the transistor comprise executing software that identifies and places the transistor in the devoid integrated-circuit region.

26. The method of claim 24 wherein placing the transistor comprises executing software that automatically places the transistor in the devoid integrated-circuit region.

27. The method of claim 24 wherein placing the transistor comprises executing software that allows one to manually place the transistor in the devoid integrated-circuit region.

28. The method of claim 24, further comprising connecting the transistor to a supply node.

29. The method of claim 24, further comprising:

identifying a conductive path; and

connecting the transistor to the path.

30. The method of claim 24, further comprising:
identifying a conductive path; and
buffering the path with the transistor.

31. The method of claim 24 wherein placing the transistor comprises placing a logic circuit in the devoid integrated-circuit region.

32. A method, comprising:
forming a circuit in a first region of an integrated circuit; and
forming a transistor in a second region of the integrated circuit, the second region being devoid of the circuit.

33. The method of claim 32, further comprising:
forming first and second supply nodes;
coupling a first terminal of the transistor to the first supply node; and
coupling second and third terminals of the transistor to the second supply node.

34. The method of claim 32, further comprising:
forming a conductive path; and
coupling first, second, and third terminals of the transistor to the conductive path.

35. The method of claim 32, further comprising:
forming a supply node;
forming a conductive path;
coupling first and second terminals of the transistor to the conductive path; and
coupling a third terminal of the transistor to the supply node.

36. The method of claim 32, further comprising:
forming first and second segments of a conductive path;
coupling an input terminal of the transistor to the first segment; and
coupling an output terminal of the transistor to the second segment.

37. The method of claim 32, further comprising:
forming first and second segments of a conductive path that is coupled to the circuit;
coupling an input terminal of the transistor to the first segment; and
coupling an output terminal of the transistor to the second segment.

38. The method of claim 32, further comprising coupling the transistor to the circuit to repair a defect in the circuit.

39. The method of claim 32, further comprising:
forming a conductive path;
dividing the conductive path into first and second uncoupled segments; and
coupling the first segment to the second segment with the transistor.

40. A method, comprising;
dividing an array into locations, the array representing an integrated-circuit;
identifying the locations in the array unoccupied by circuit blocks; and
placing transistors in the unoccupied locations.

41. The method of claim 40 wherein placing transistors comprises placing blocks of transistors in the unoccupied locations.

42. A method of integrating additional transistors into an integrated circuit, the method comprising:
calculating the dimensions of an array to store validity data;
initializing the array as valid;
reading block information including location and dimensions;
calculating the locations in the validity array corresponding to the block location and dimensions;
marking the locations in the validity array as invalid;
checking for more blocks;
if more blocks are found, looping back to the step of reading block information;
if no more blocks are found, continuing:
for each location in the validity array, if valid, then place a transistor array block;
else, continue to next location.

43. The method of claim 42, further comprising allowing a user to invalidate locations within the validity array.